

FPGA Tile 20

10066539.013002

FIG. 1

10066539.013002

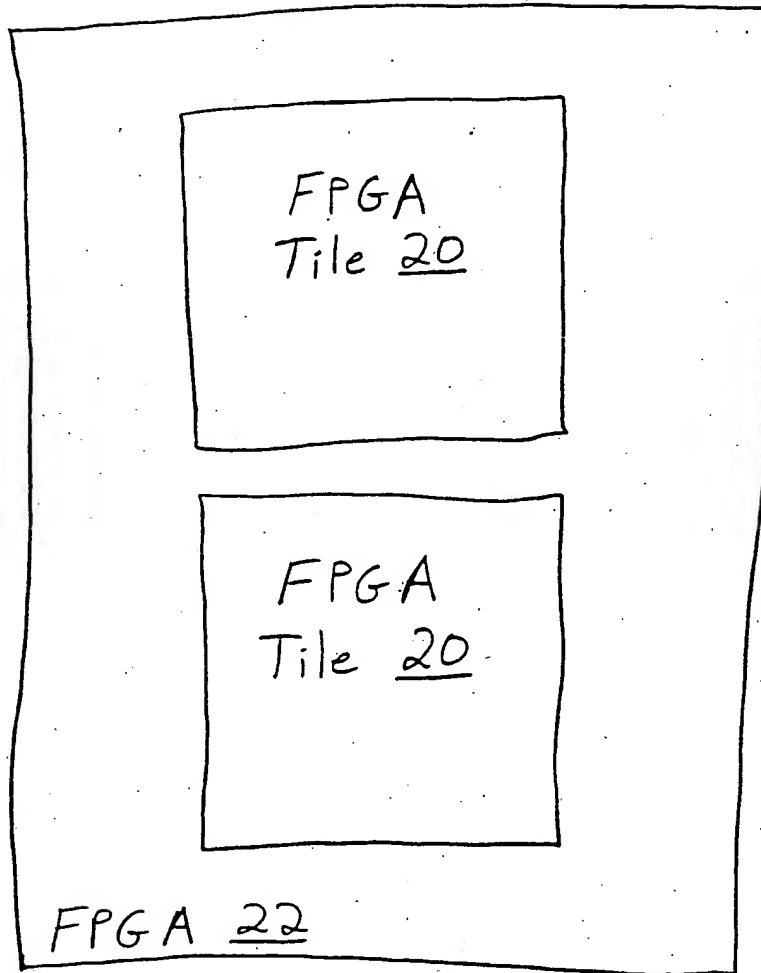


FIG. 2

20060659.013002

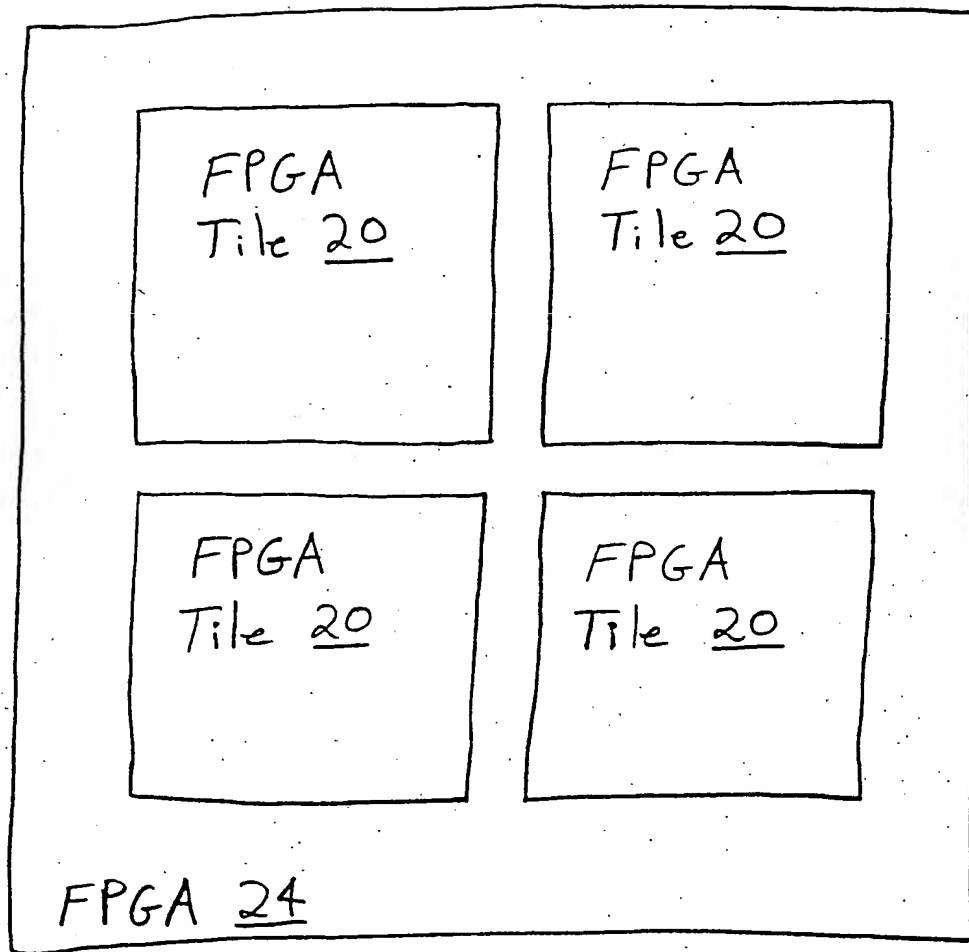


FIG. 3A

10066539.013002

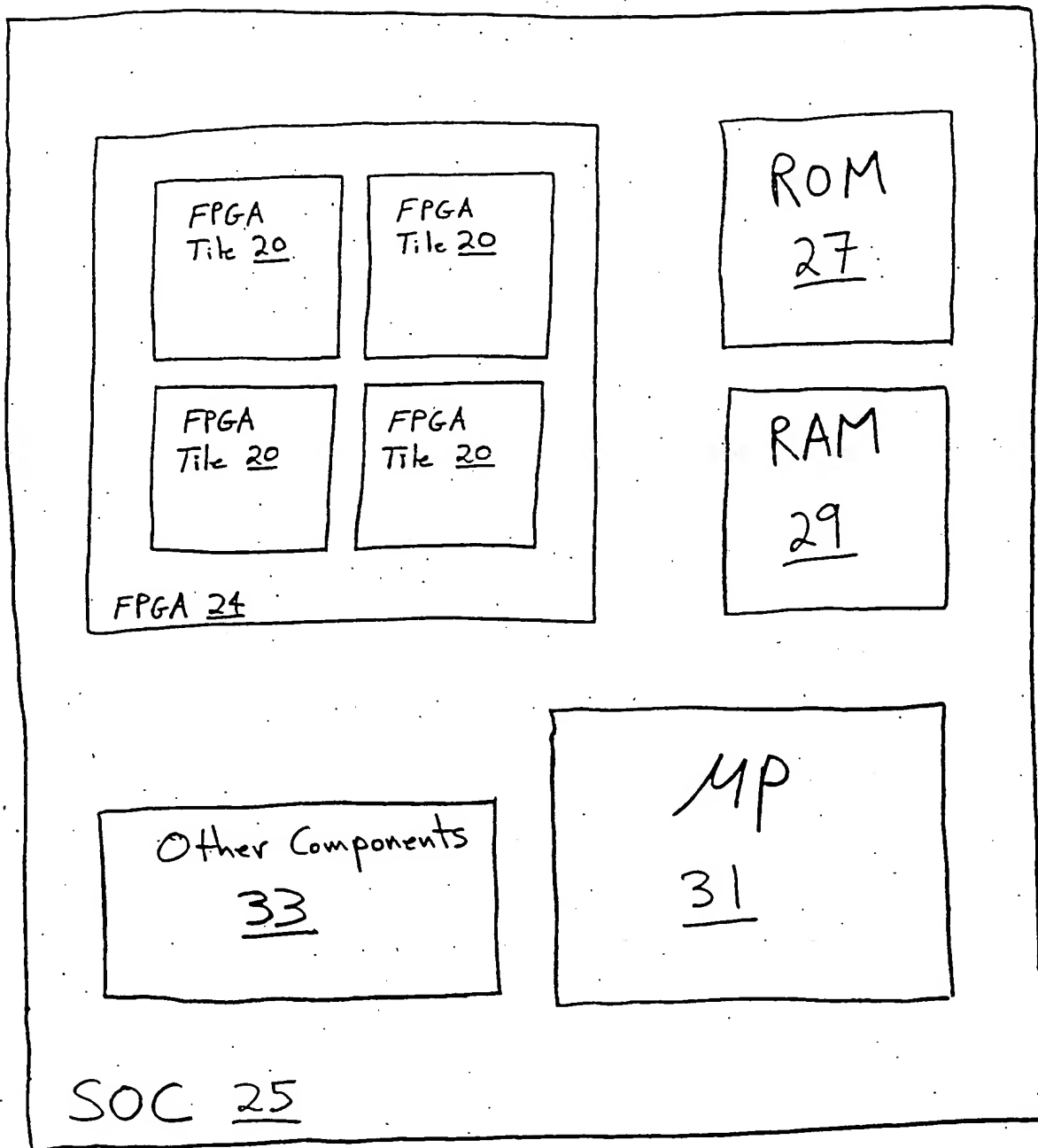
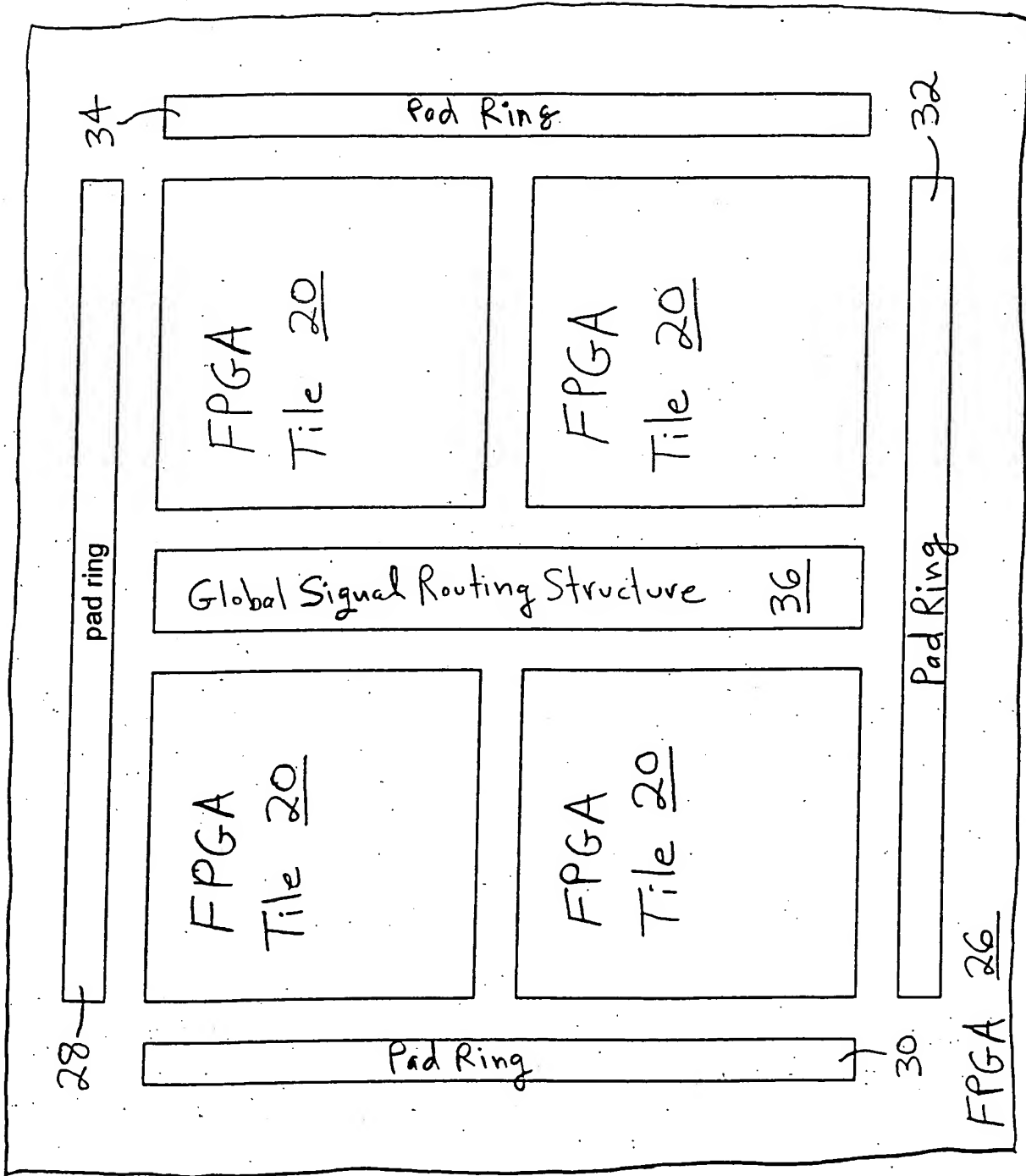


FIG. 3B

200610 6659001



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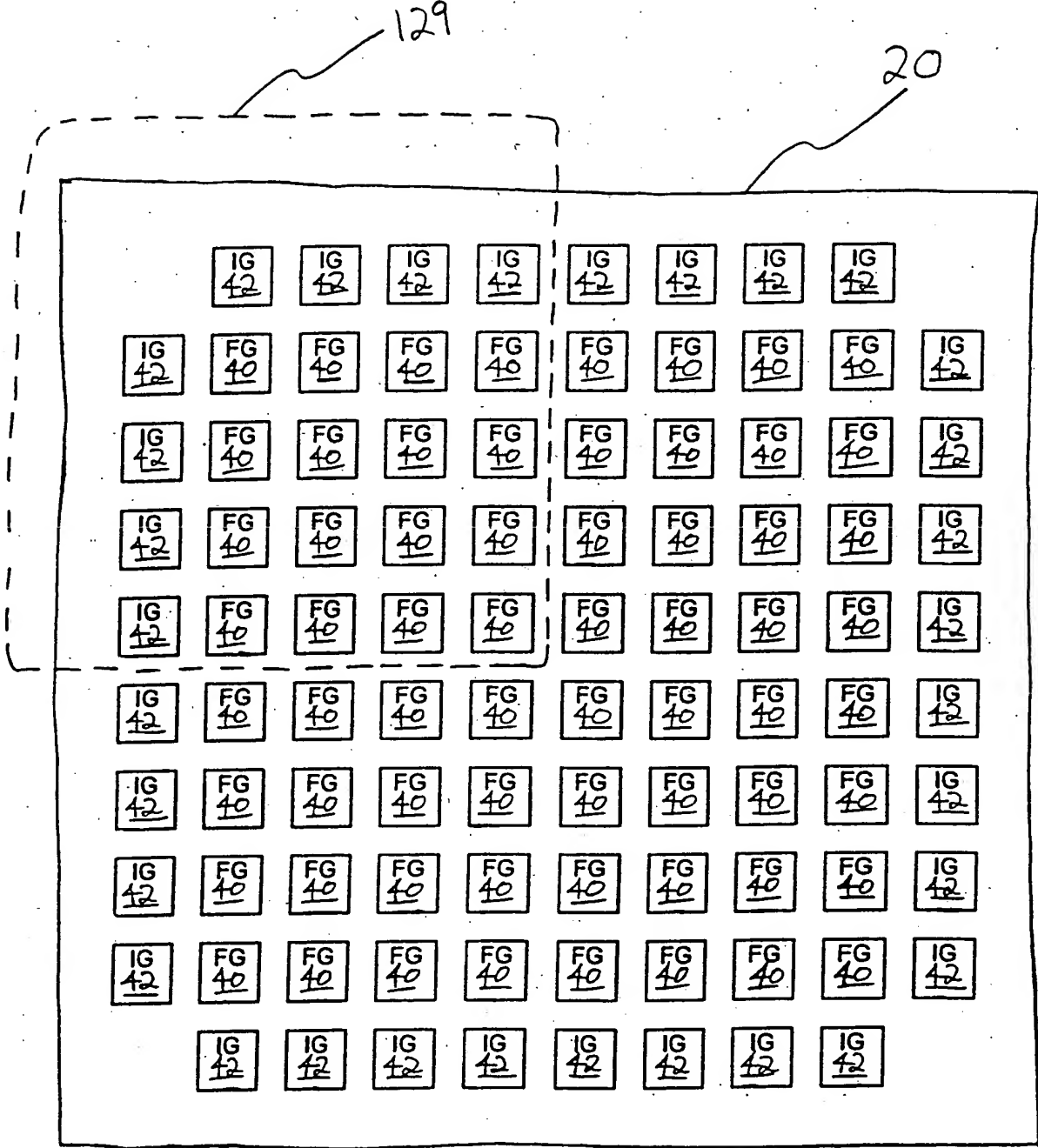


FIG. 5

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200610-66699007

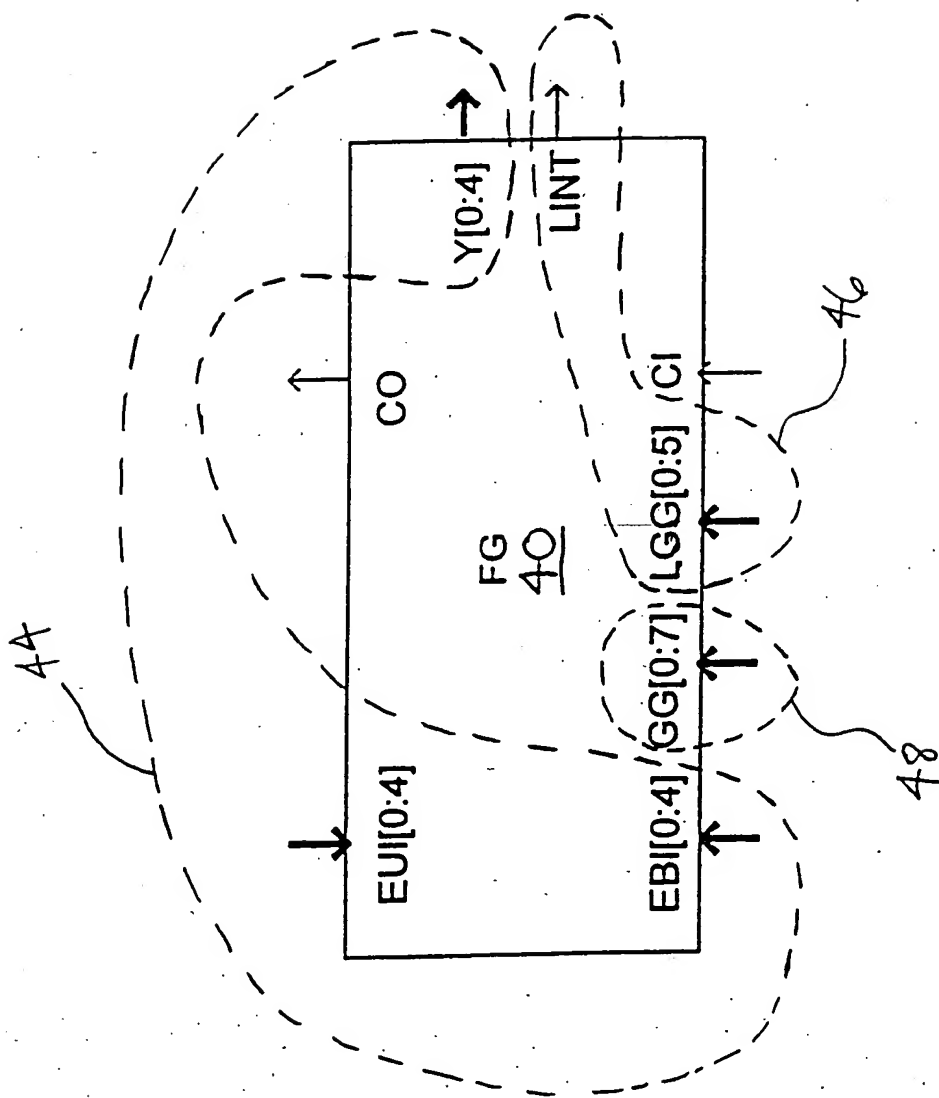
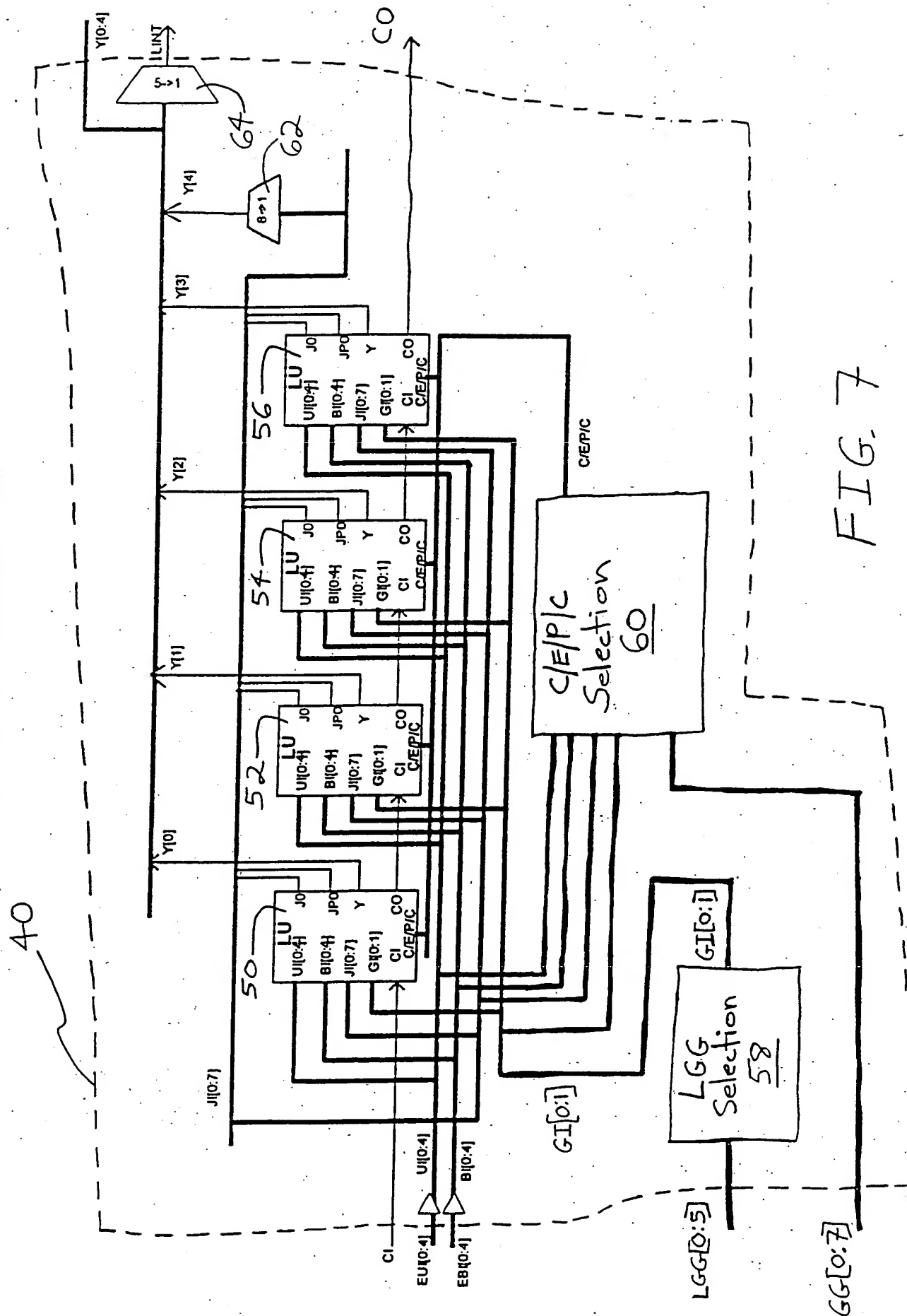


FIG. 6

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ACT-317

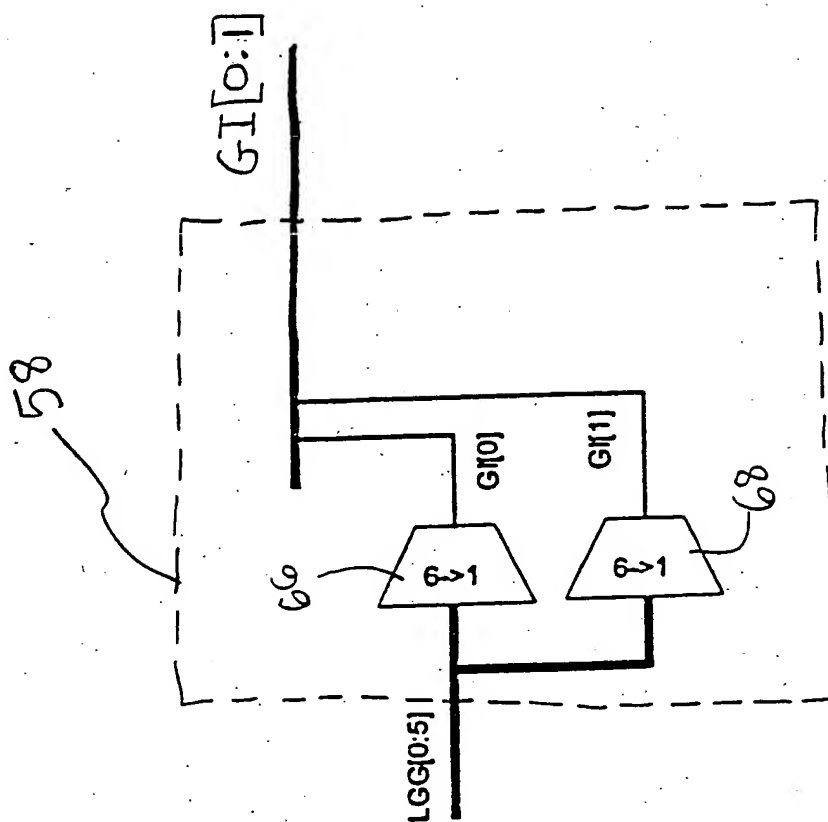


FIG. 8

200606599001

20050105599001

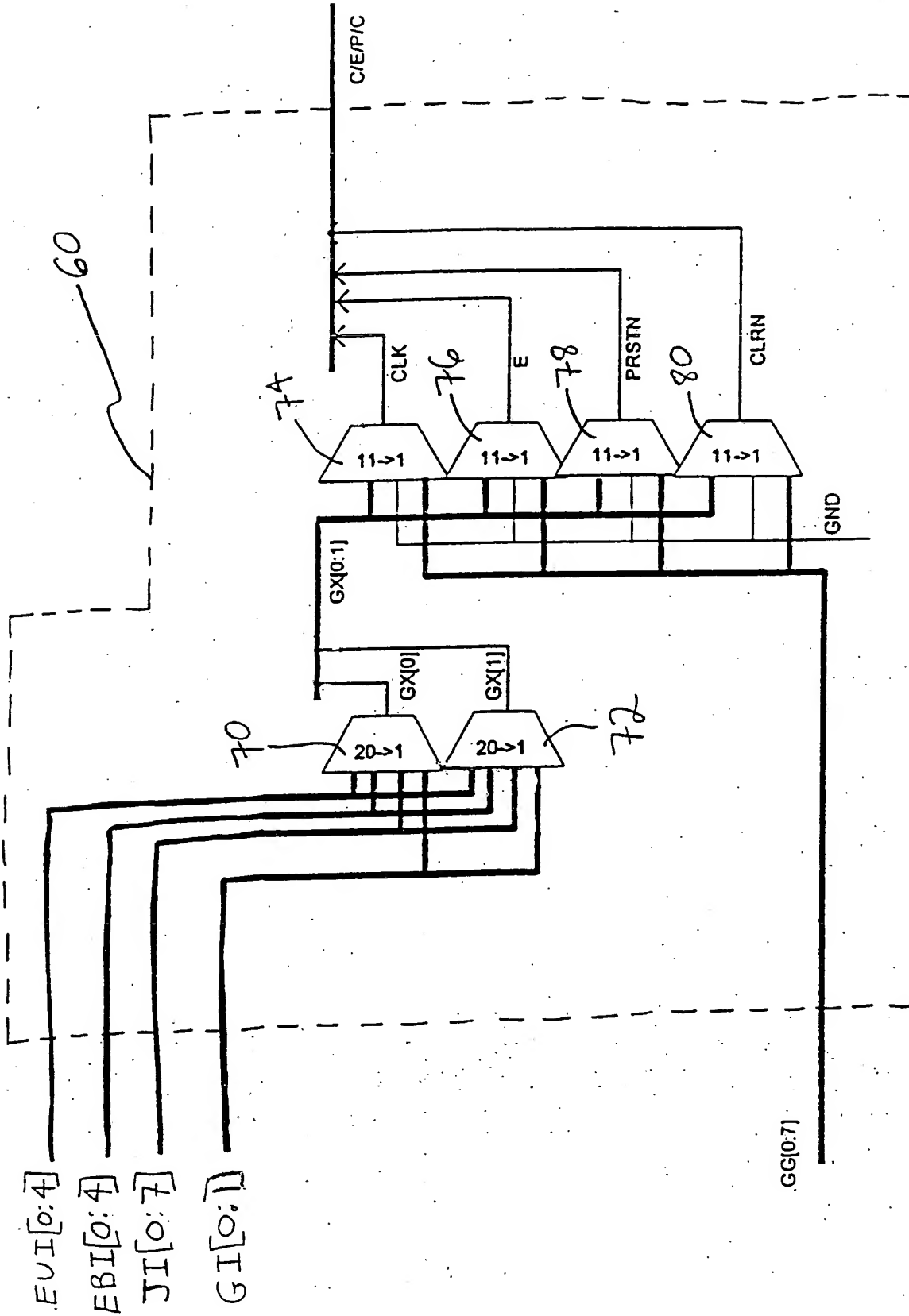


FIG. 9

200510 55599001

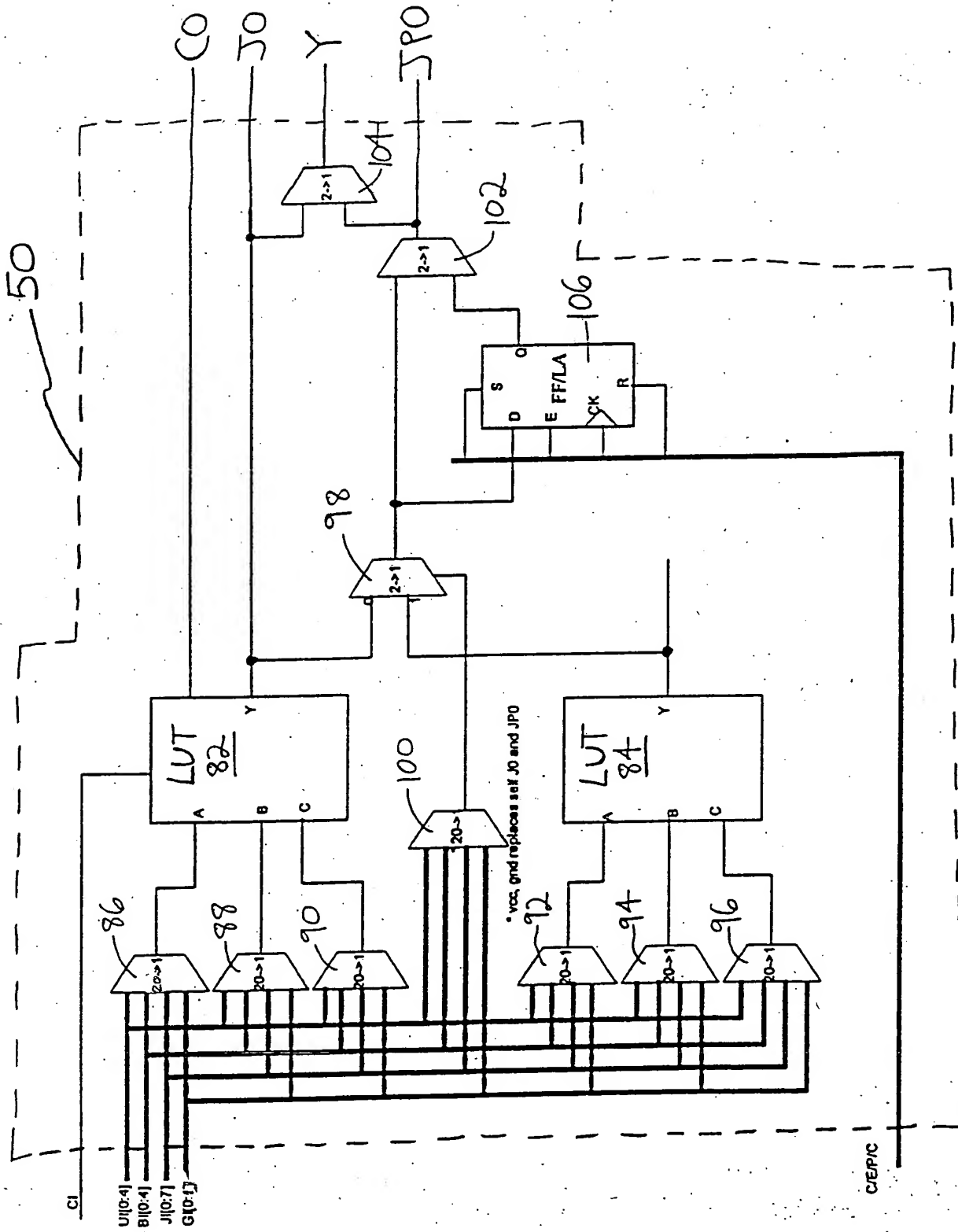


FIG. 10

200610-55599001

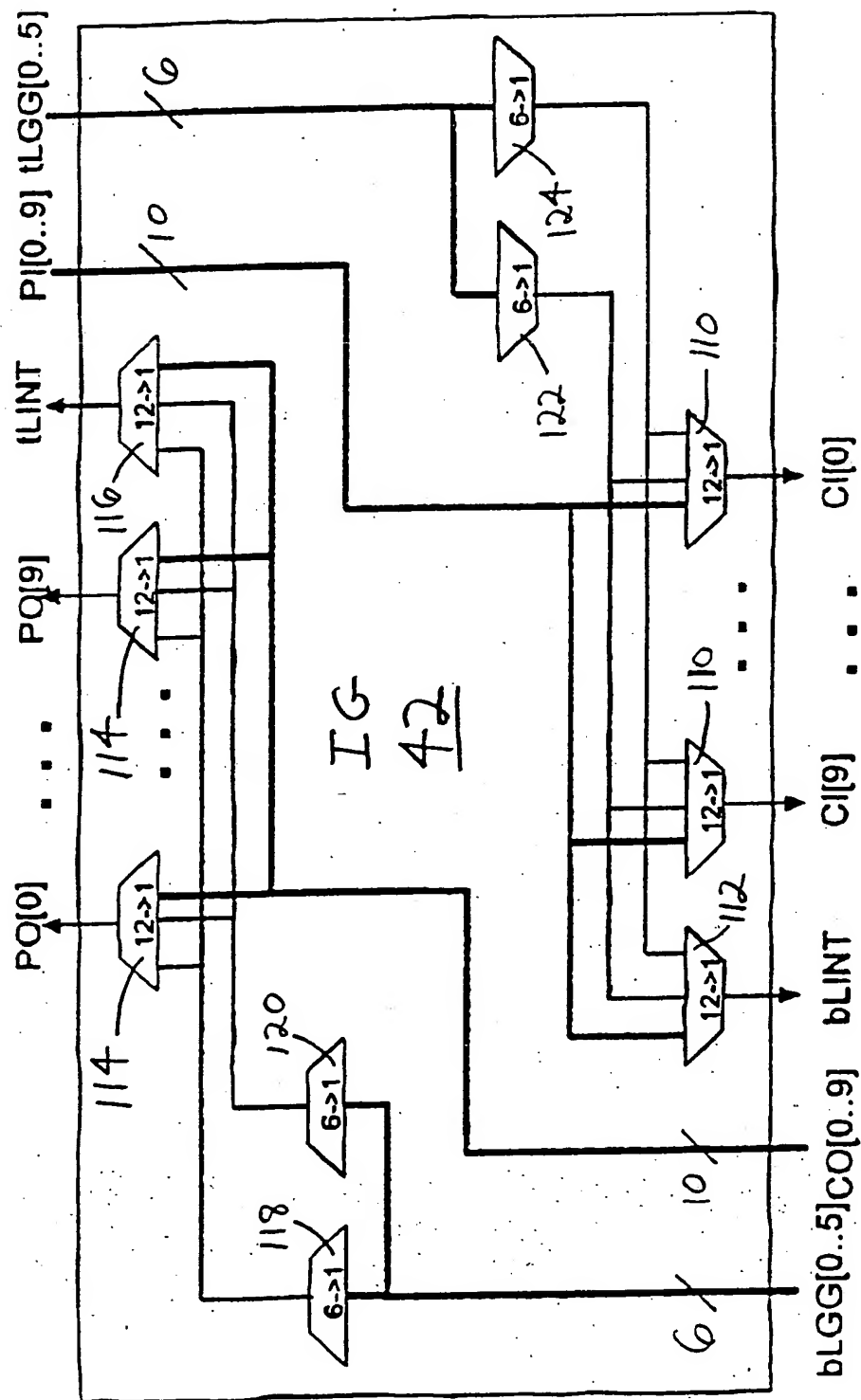
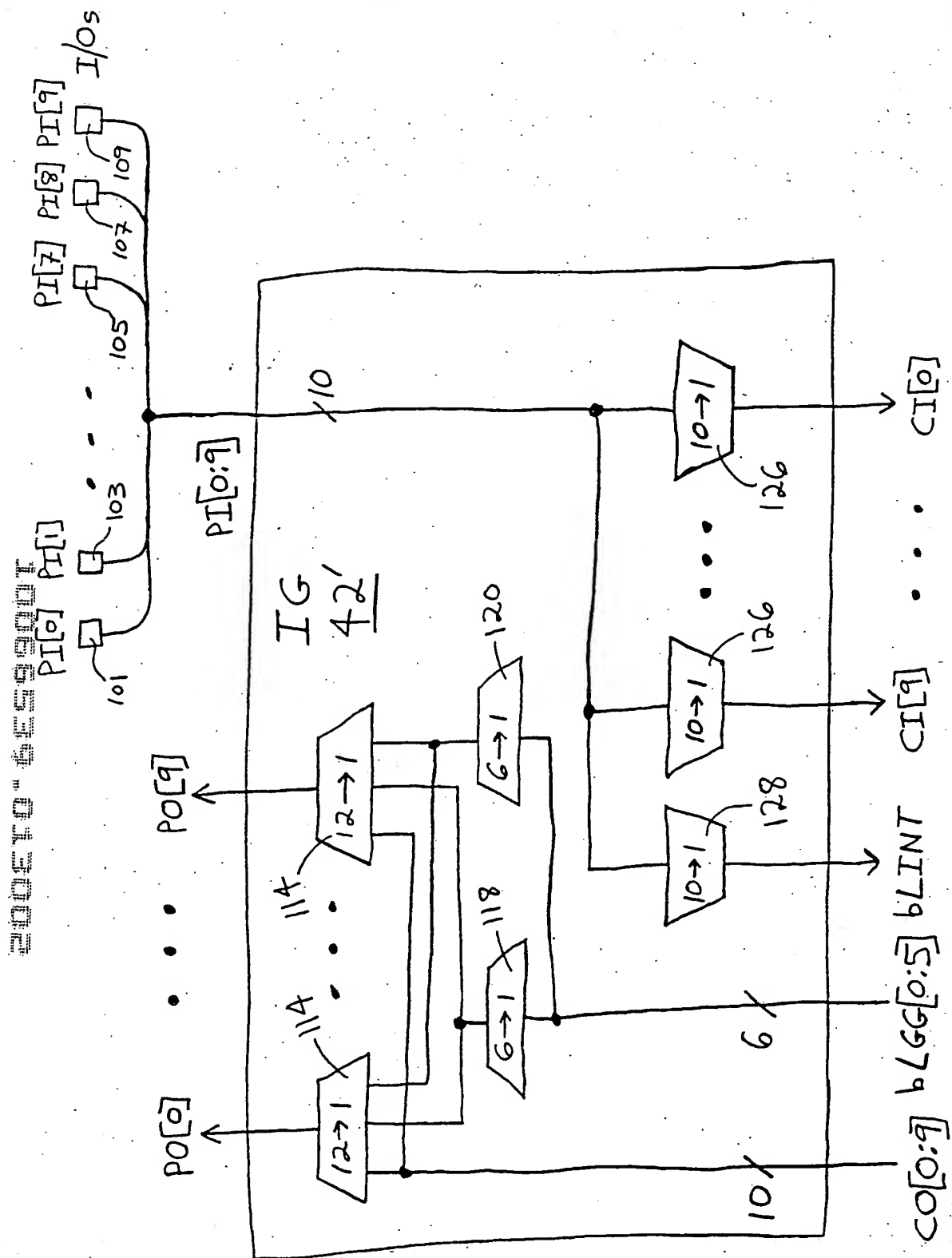
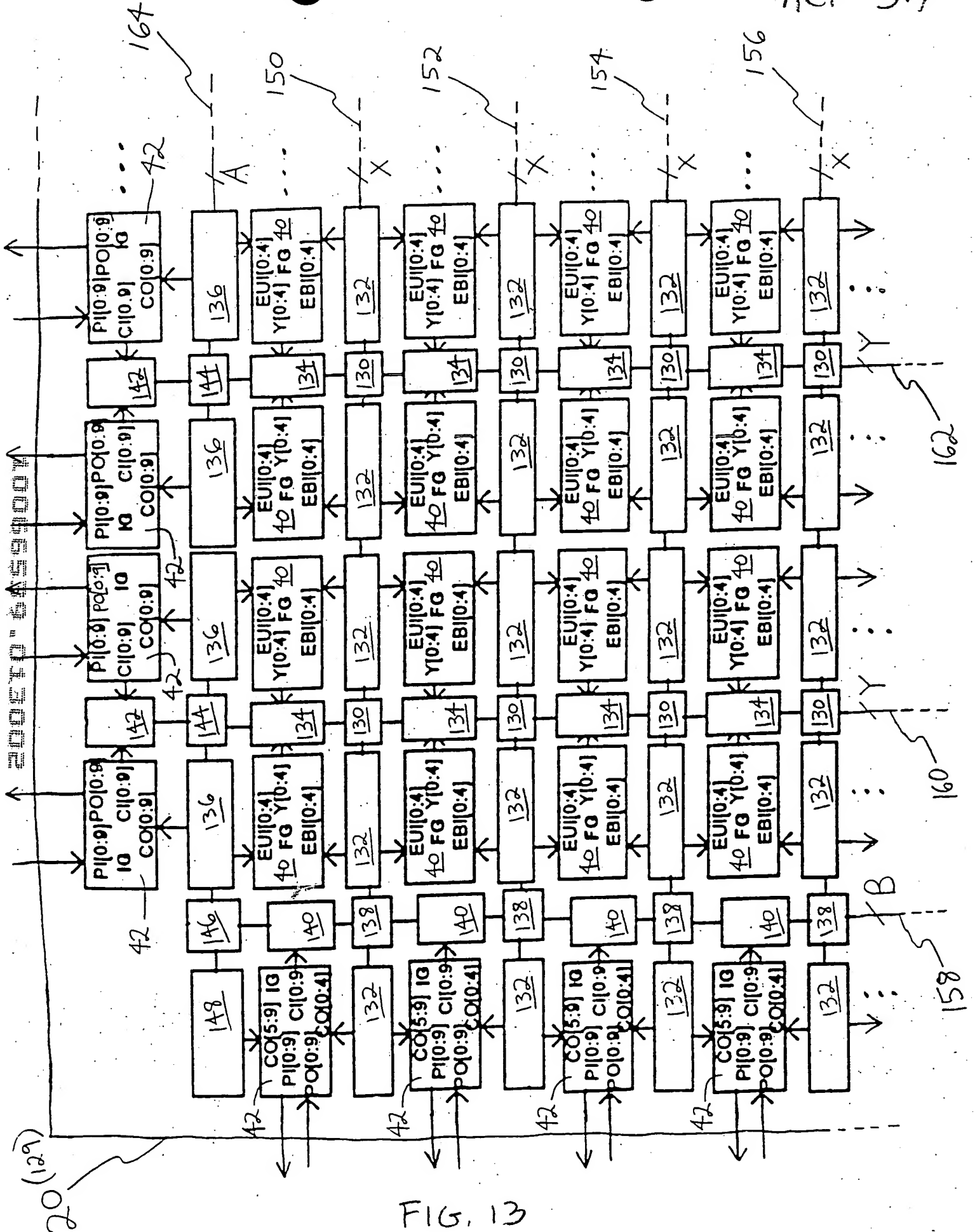


FIG. 11

ACT-317



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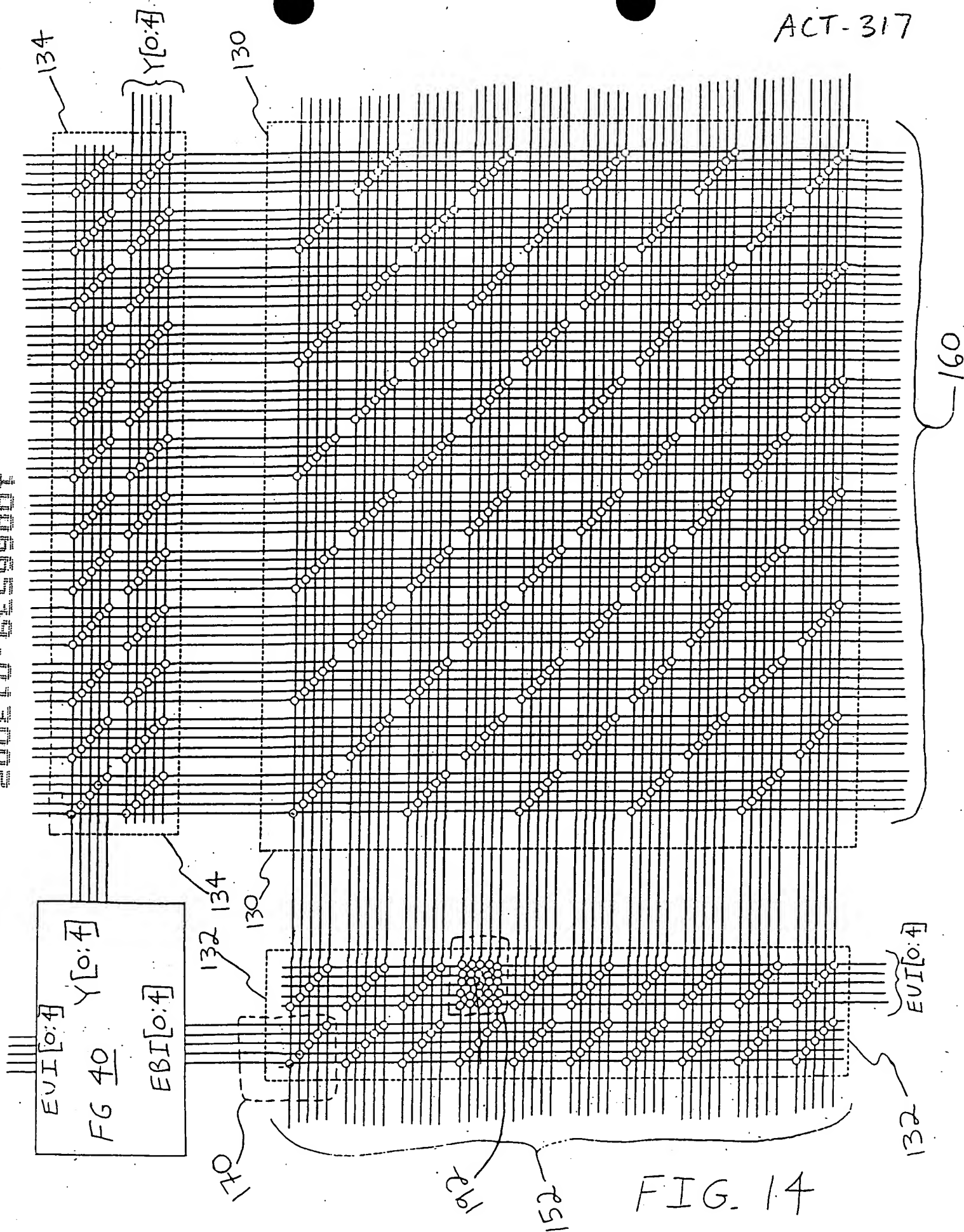


FIG. 14

ACT-317

2006539-040007

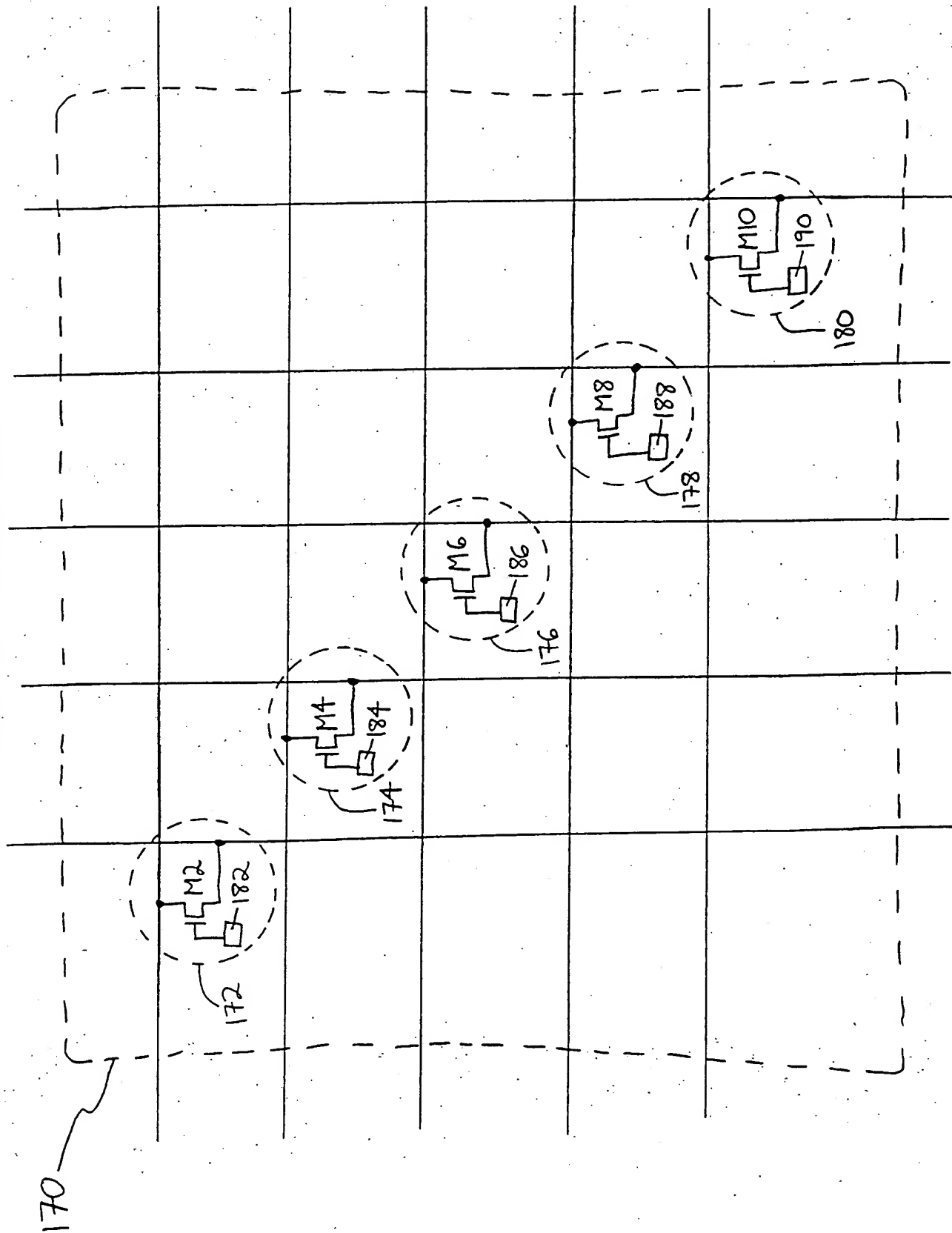


FIG. 15

10066537-013002

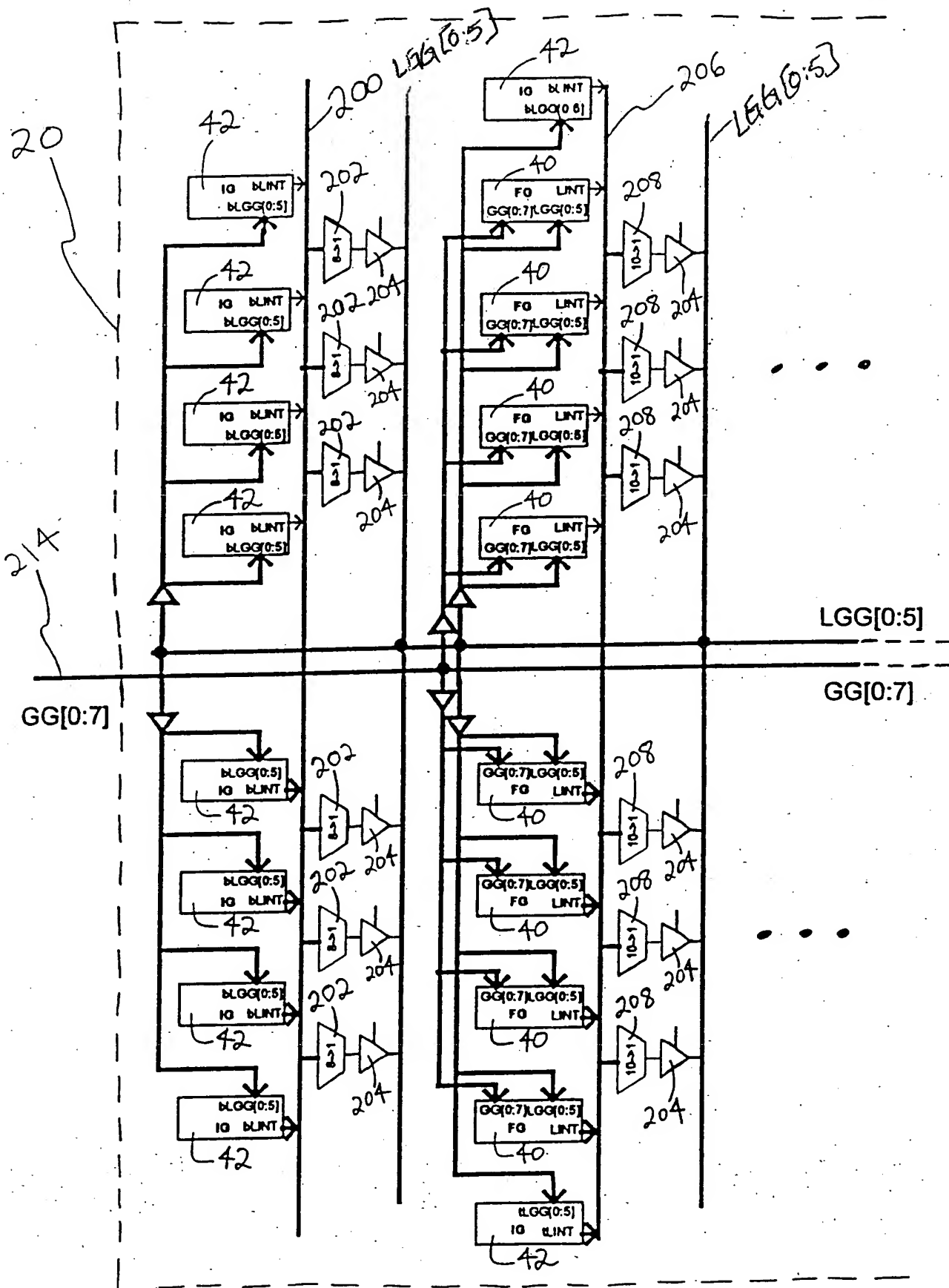


FIG. 16A

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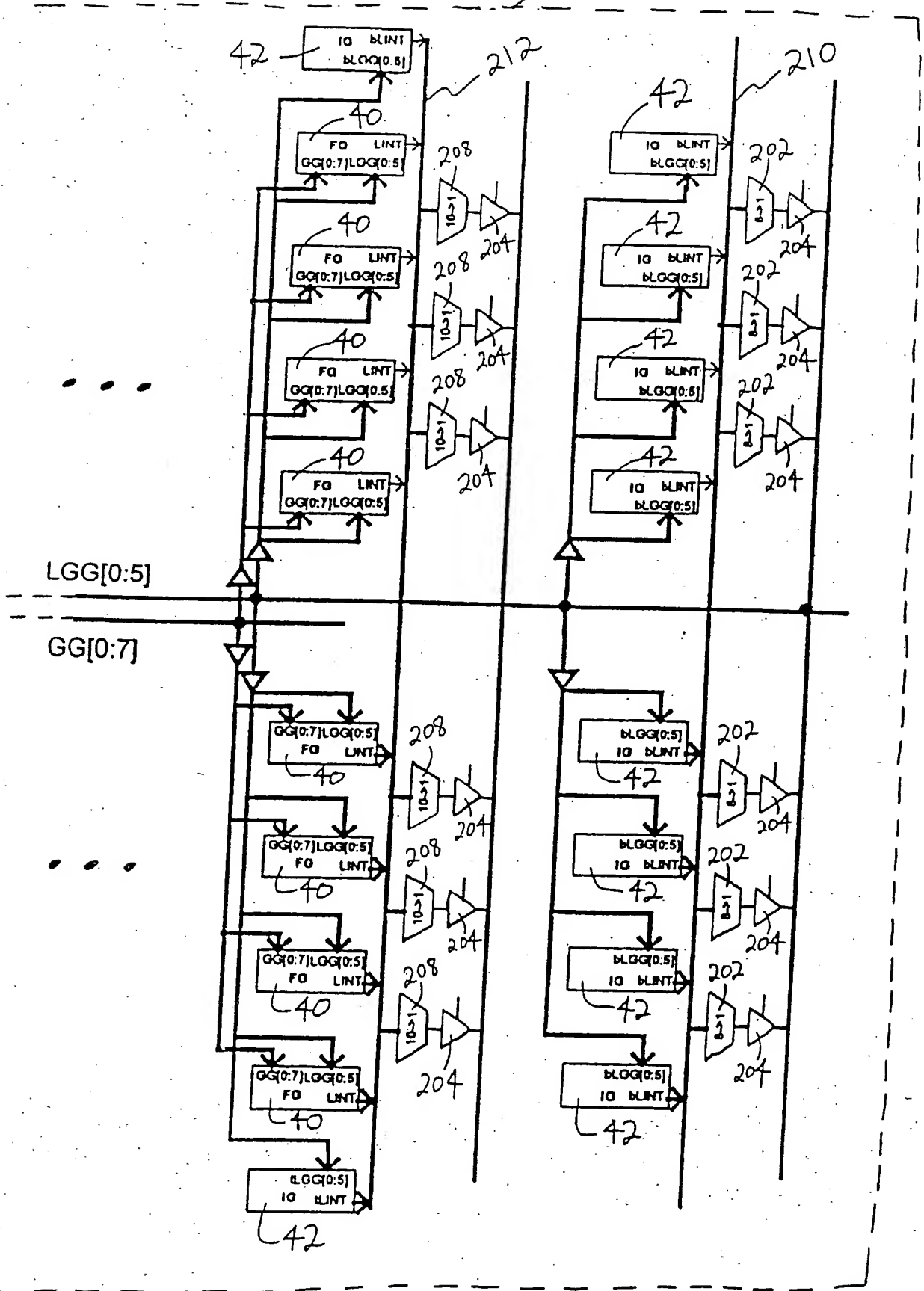


FIG. 16B

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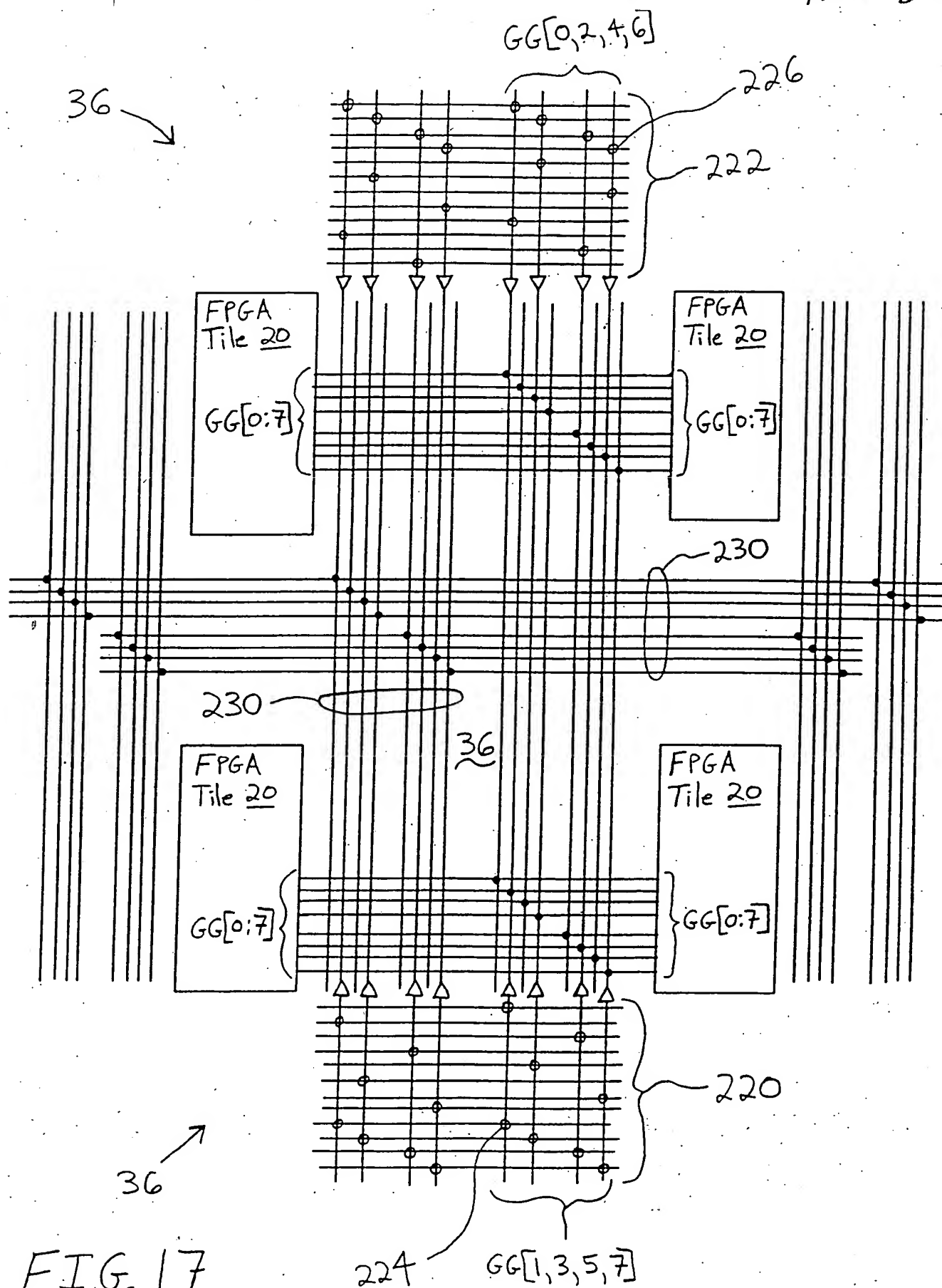


FIG. 17

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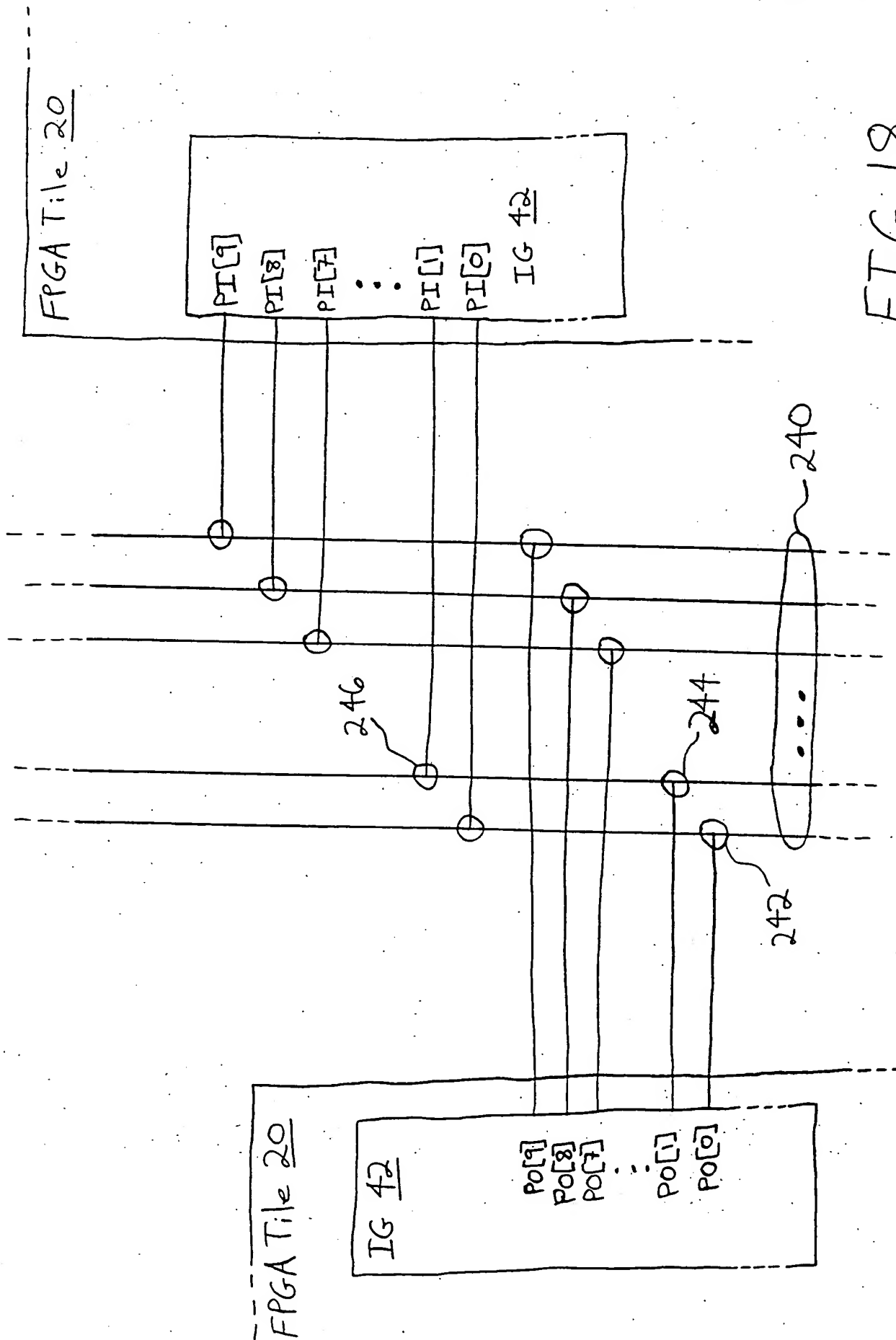


FIG. 18

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Vertical Track Testing Circuit

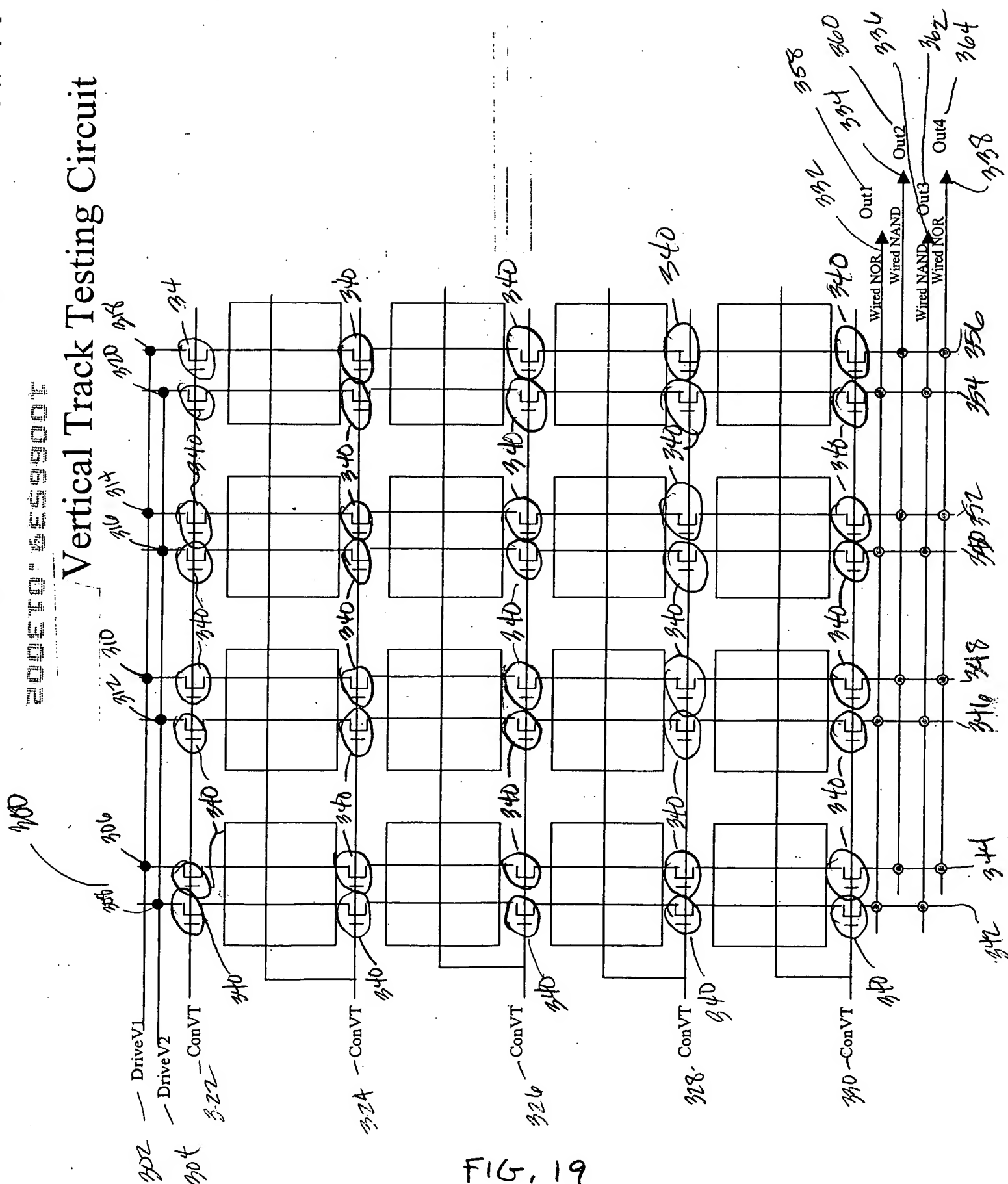


FIG. 19

Truth Table

DriveV1	DriveV2	Out1	Out2	Out3	Out4
0	0	1	1	1	1
0	1	1	0	1	0
1	0	0	1	0	1
1	1	0	0	0	0

Fig. 20

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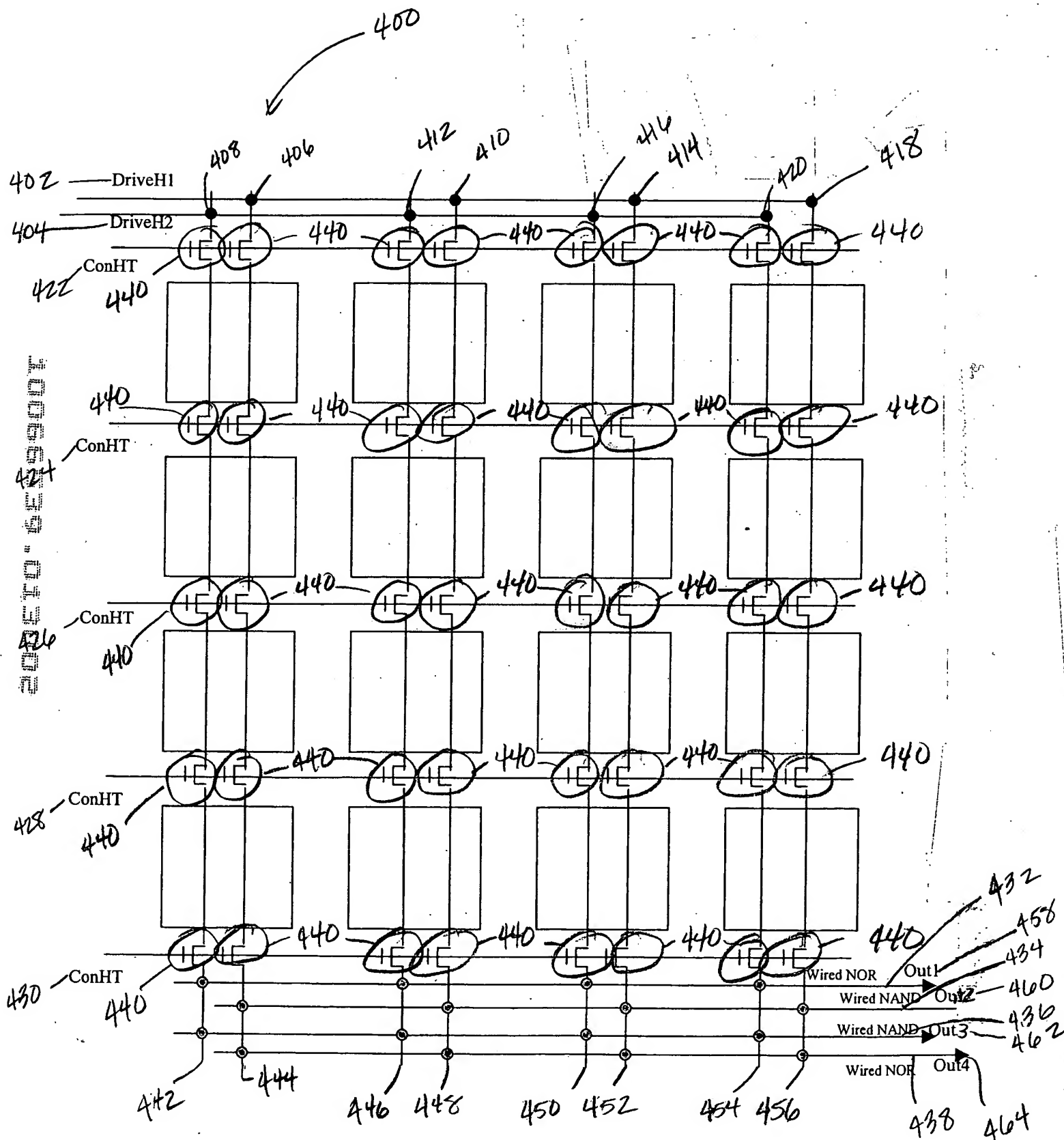


FIG. 21

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Truth Table

DriveH1	DriveH2	Out1	Out2	Out3	Out4
0	0	1	1	1	1
0	1	1	0	1	0
1	0	0	1	0	1
1	1	0	0	0	0

FIG. 22